FIG. 1a

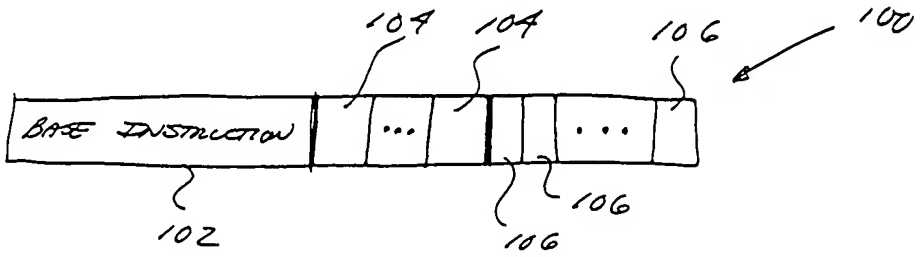


FIG. 1b

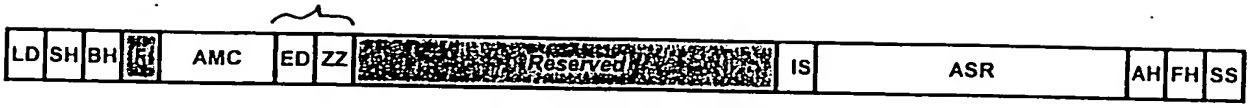


Fig. 1c

190

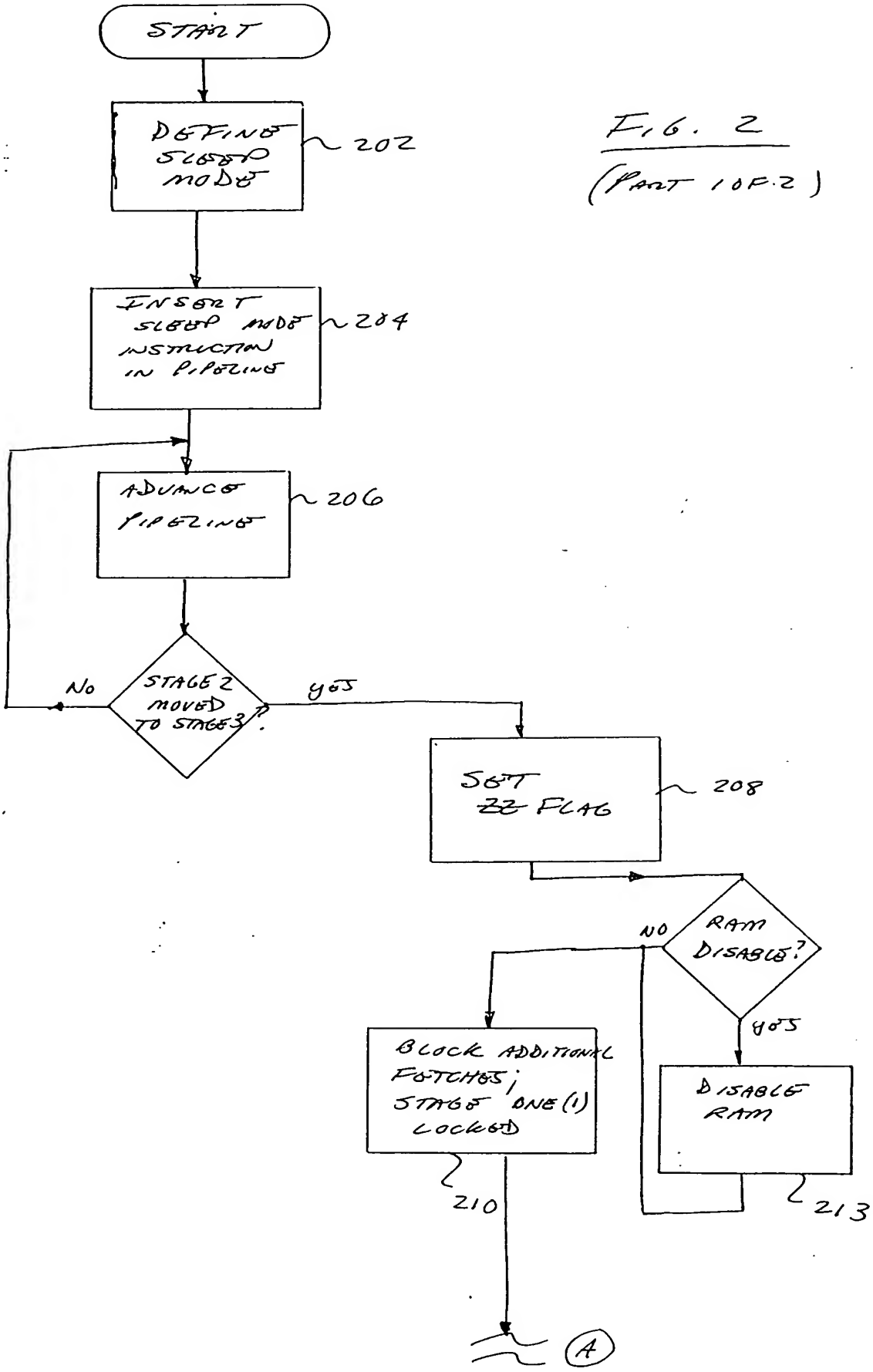


FIG. 2
(PART 1 OF 2)

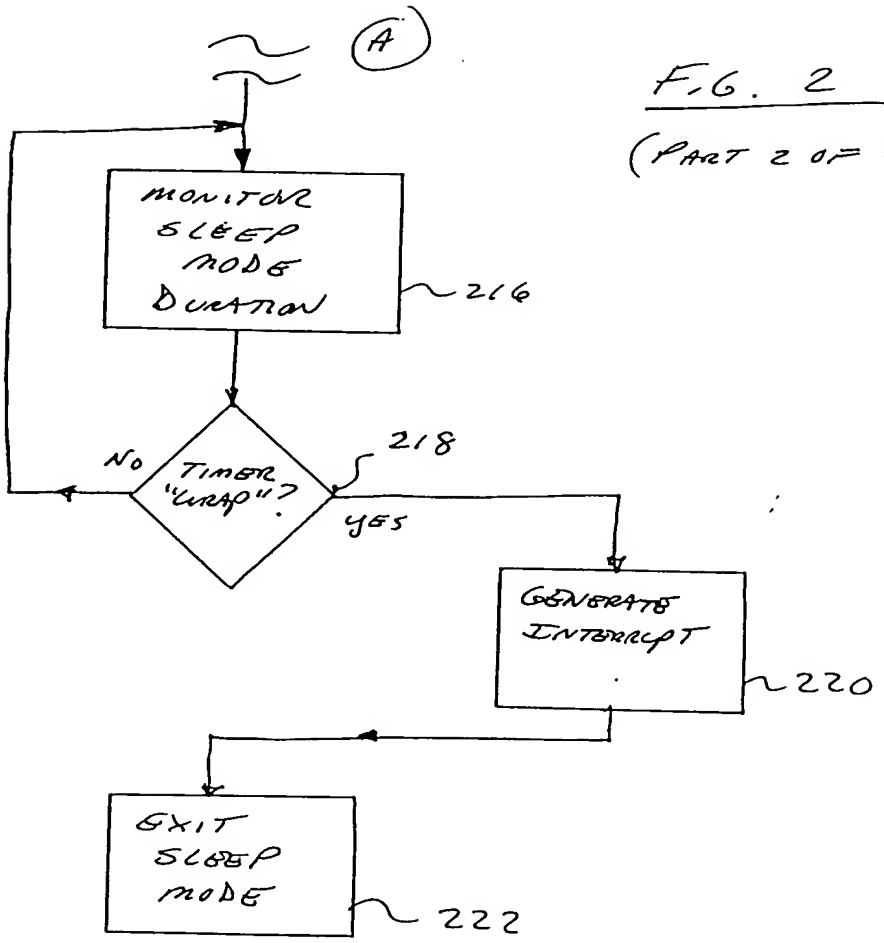


FIG. 2
(PART 2 OF 2)

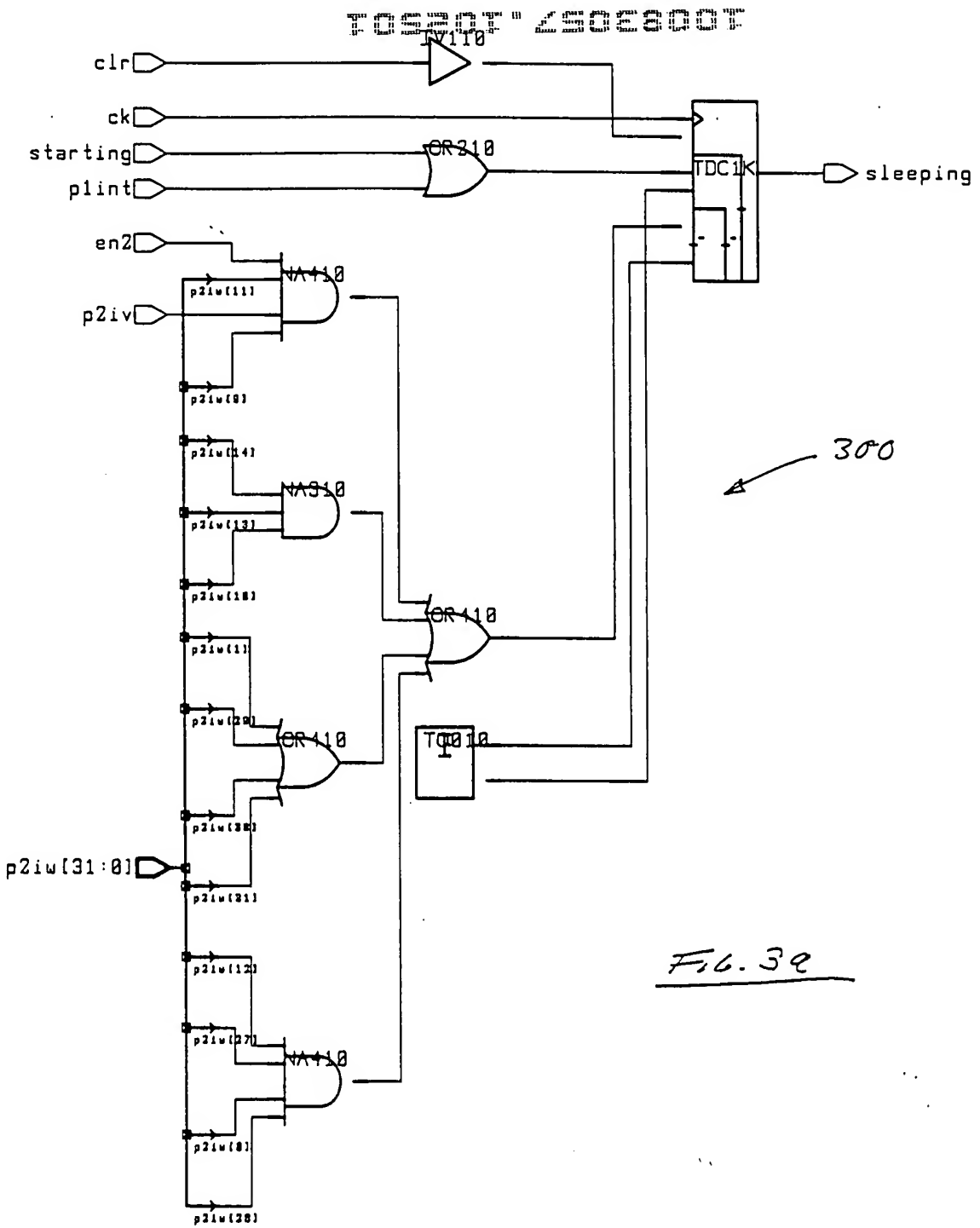


FIG. 3a

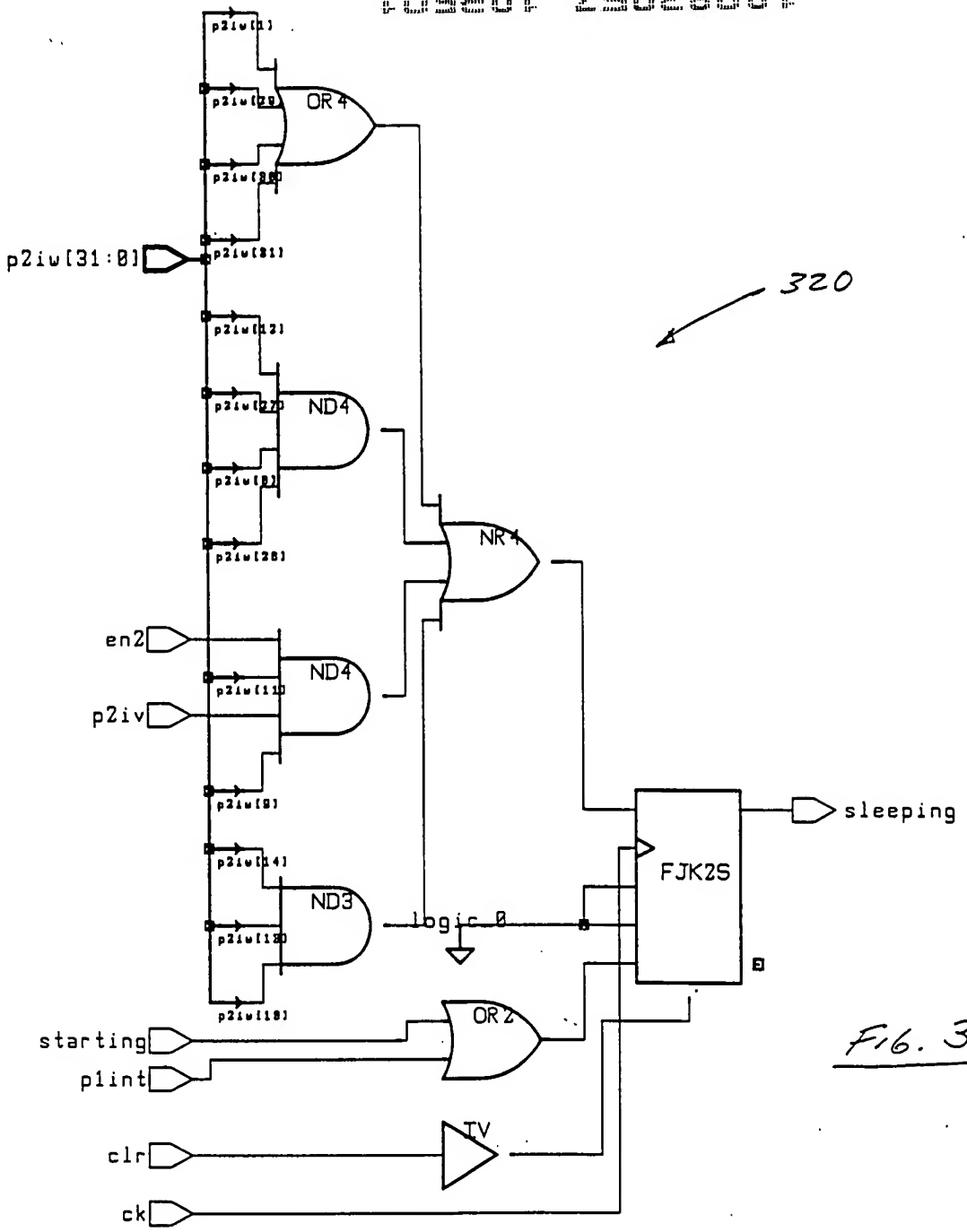

p2iw[31:0]
OR4
ND4
ND4
ND3
NR4
en2
p2iv
logic 0
FJK2S
sleeping
OR2
starting
p1int
IV
clr
ck
320

Fig. 3b

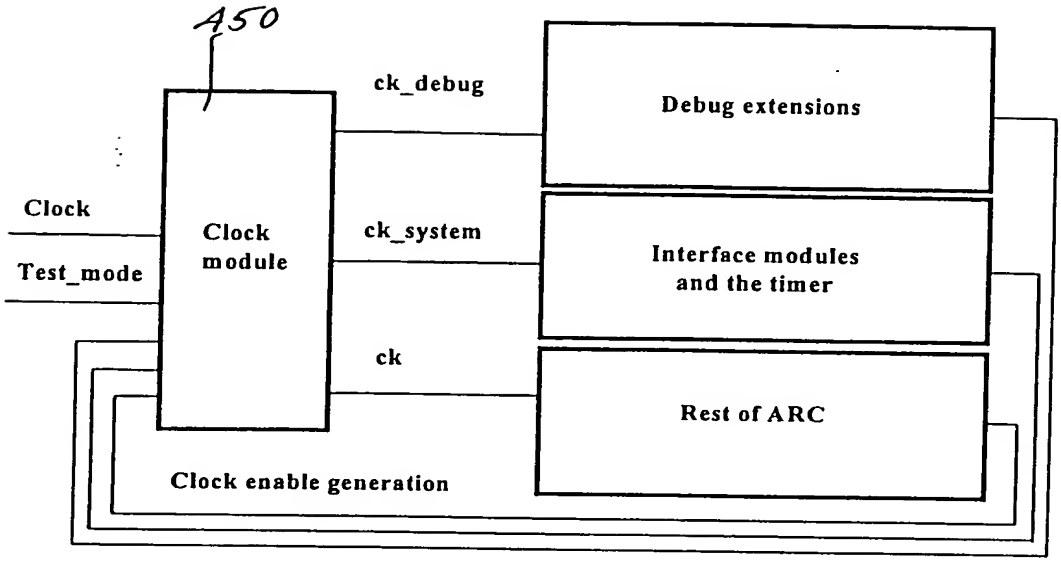

450
ck_debug
Debug extensions
Clock
Clock module
ck_system
Test_mode
Interface modules and the timer
ck
Rest of ARC
Clock enable generation

Fig. 4a

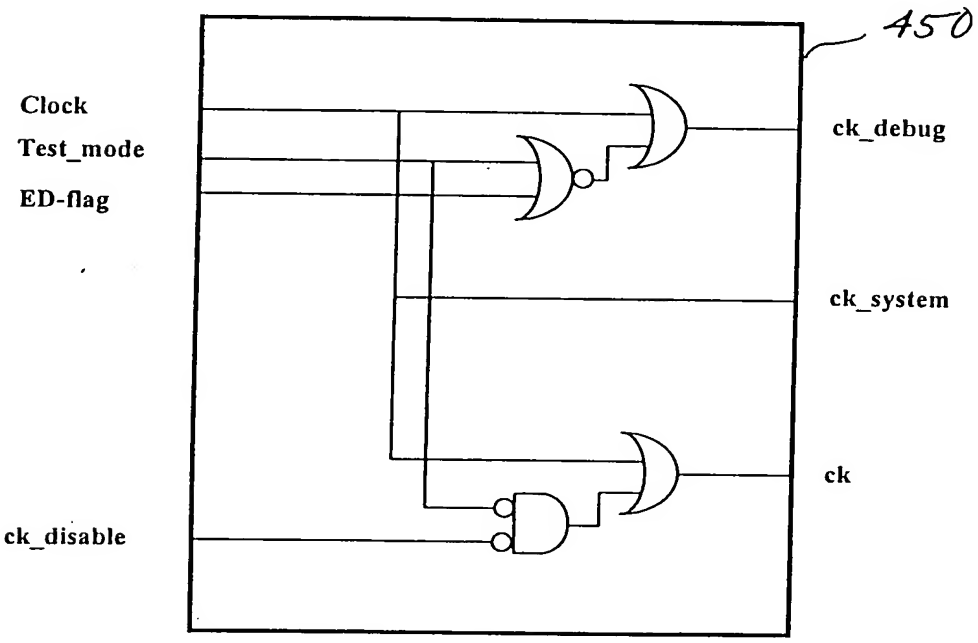

450
Clock
Test_mode
ED-flag
ck_debug
ck_system
ck
ck_disable

Fig. 4b

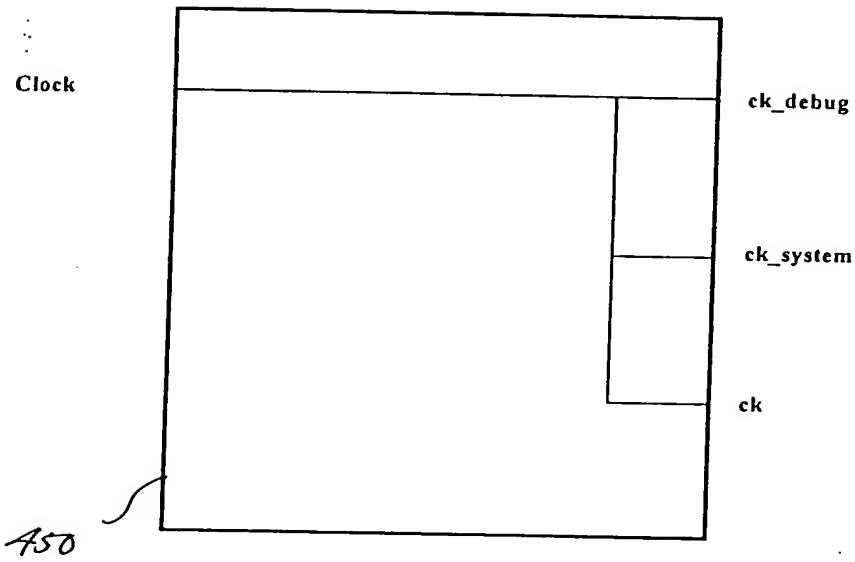
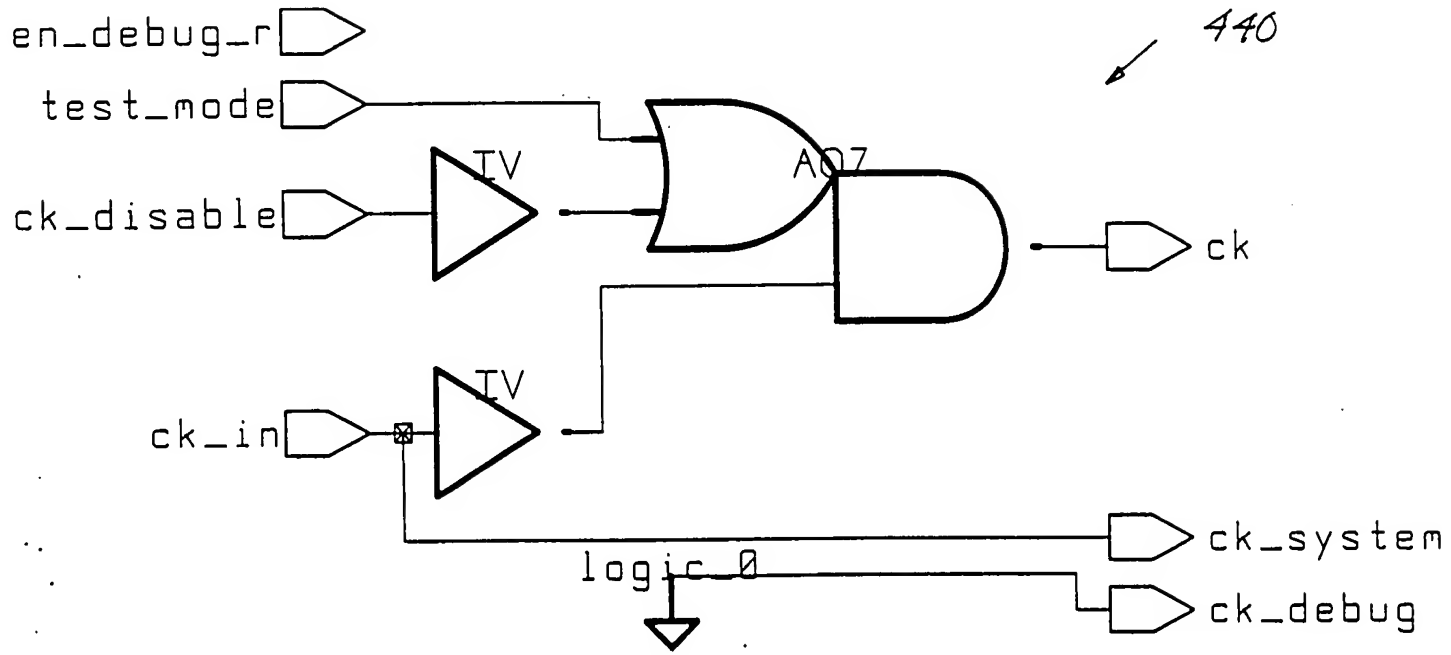


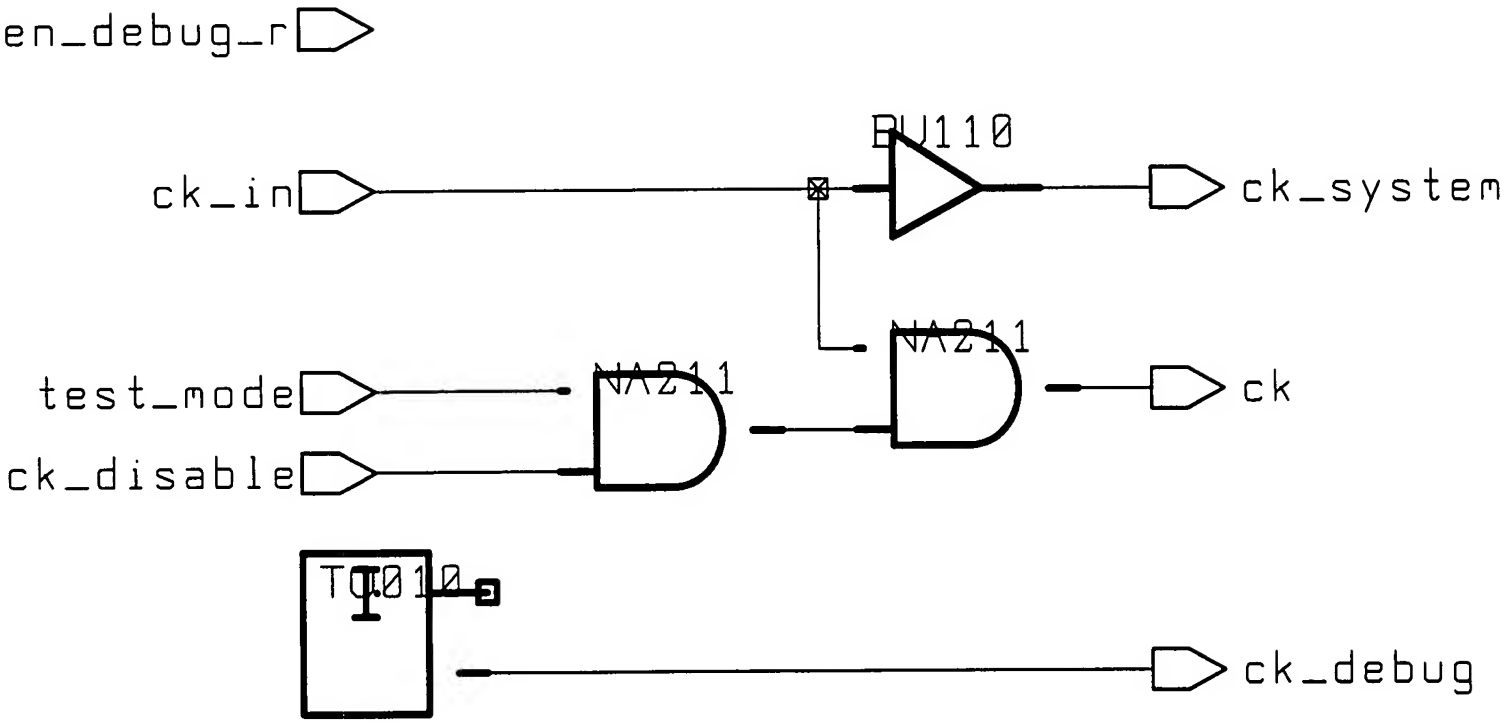
Fig. 4c

Fig. 4d


en_debug_r
test_mode
ck_disable
ck_in
TV
TV
AO7
440
ck
ck_system
logic_0
ck_debug

460

Fig. 4e


en_debug_r
BU110
ck_in
ck_system
NA211
NA211
test_mode
ck
ck_disable
TI010
ck_debug

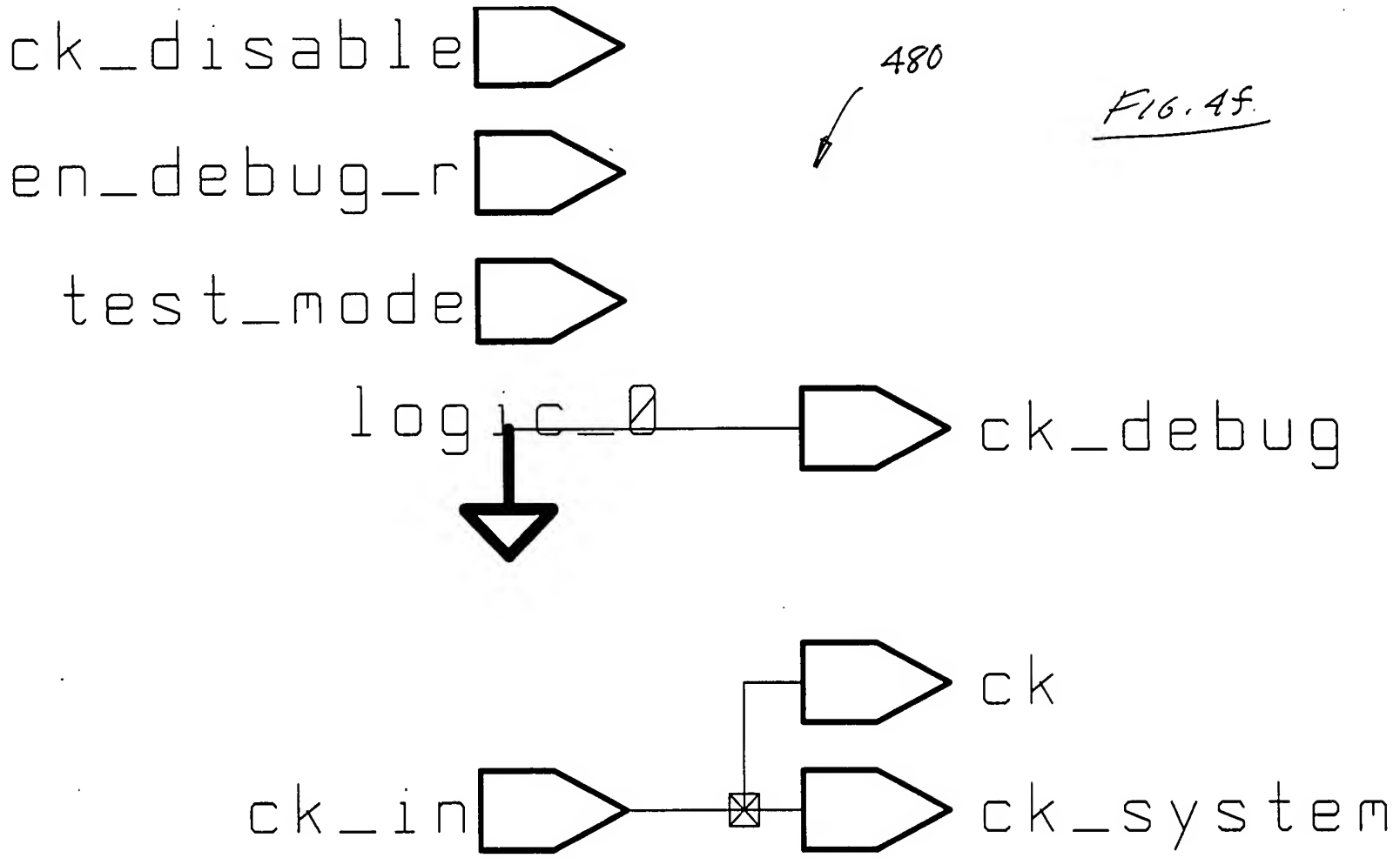

ck_disable
en_debug_r
test_mode
logic_0
ck_debug
ck
ck_in
ck_system
480

Fig. 4f

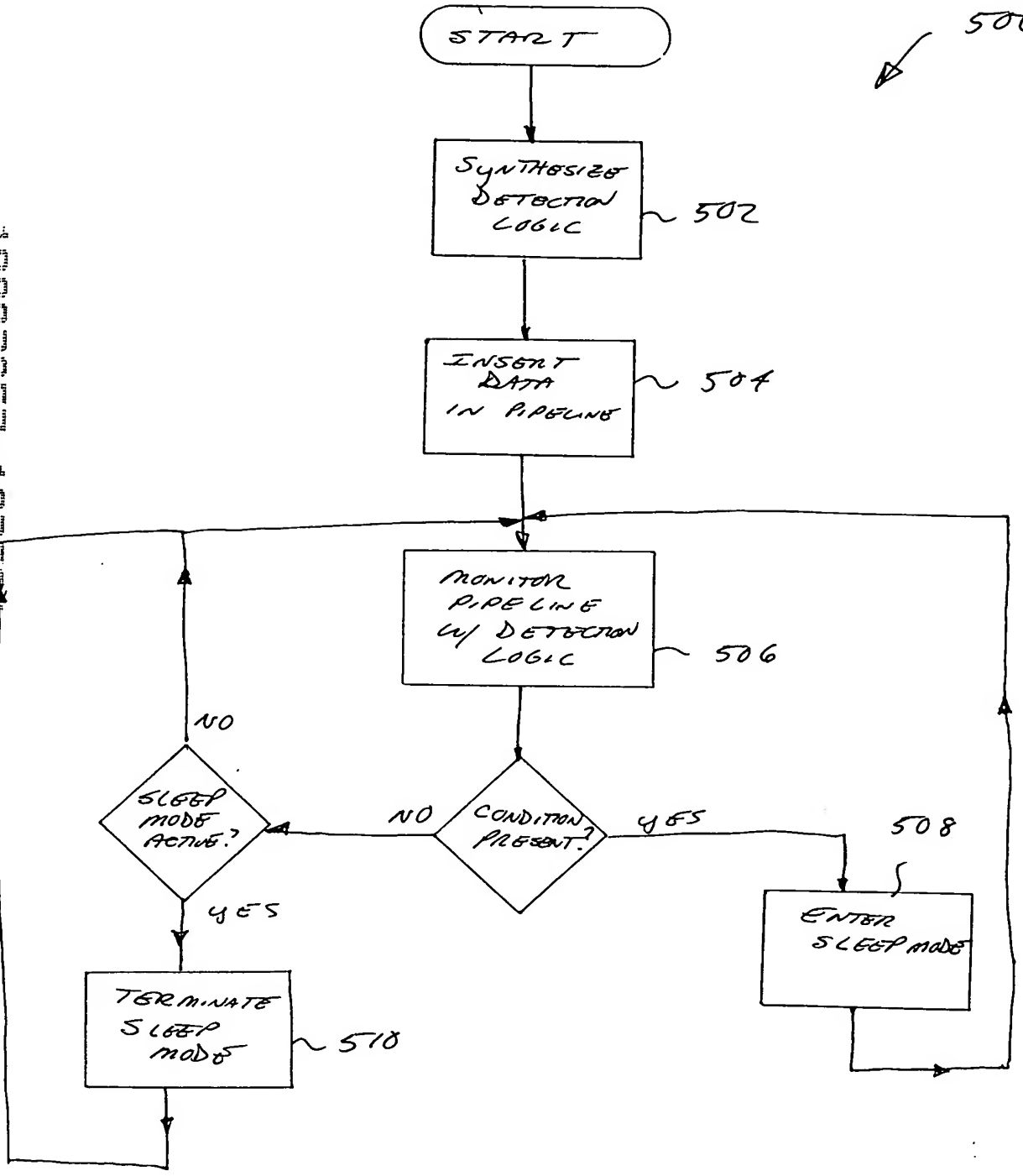

500
START
SYNTHESIZE DETECTION LOGIC
502
INSERT DATA IN PIPELINE
504
MONITOR PIPELINE W/ DETECTION LOGIC
506
CONDITION PRESENT?
YES
NO
508
ENTER SLEEP MODE
SLEEP MODE ACTIVE?
NO
YES
TERMINATE SLEEP MODE
510

FIG. 5

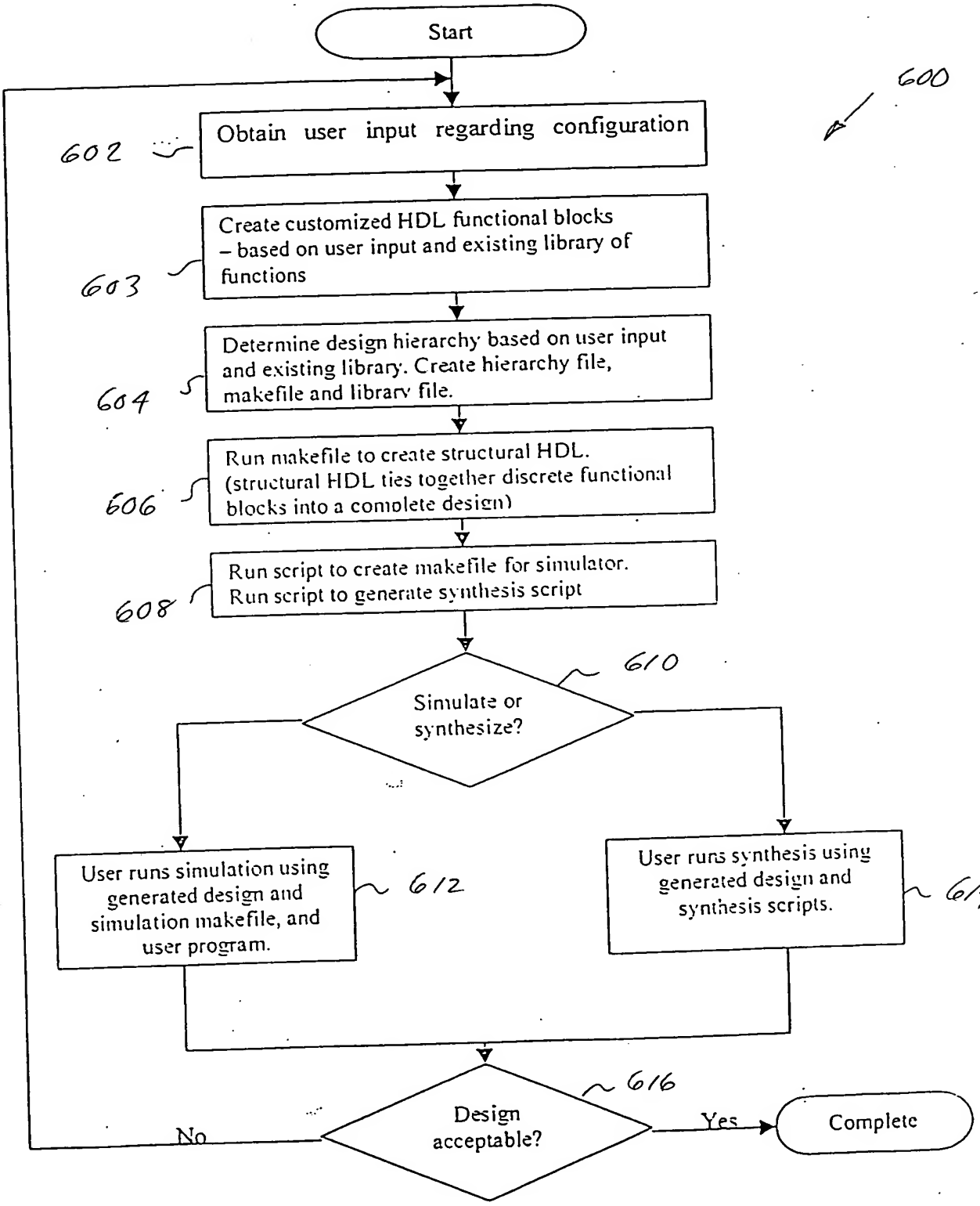

Start
600
602
Obtain user input regarding configuration
603
Create customized HDL functional blocks – based on user input and existing library of functions
604
Determine design hierarchy based on user input and existing library. Create hierarchy file, makefile and library file.
606
Run makefile to create structural HDL. (structural HDL ties together discrete functional blocks into a complete design)
608
Run script to create makefile for simulator. Run script to generate synthesis script
610
Simulate or synthesize?
User runs simulation using generated design and simulation makefile, and user program.
612
User runs synthesis using generated design and synthesis scripts.
614
616
Design acceptable?
No
Yes
Complete

FIG. 6

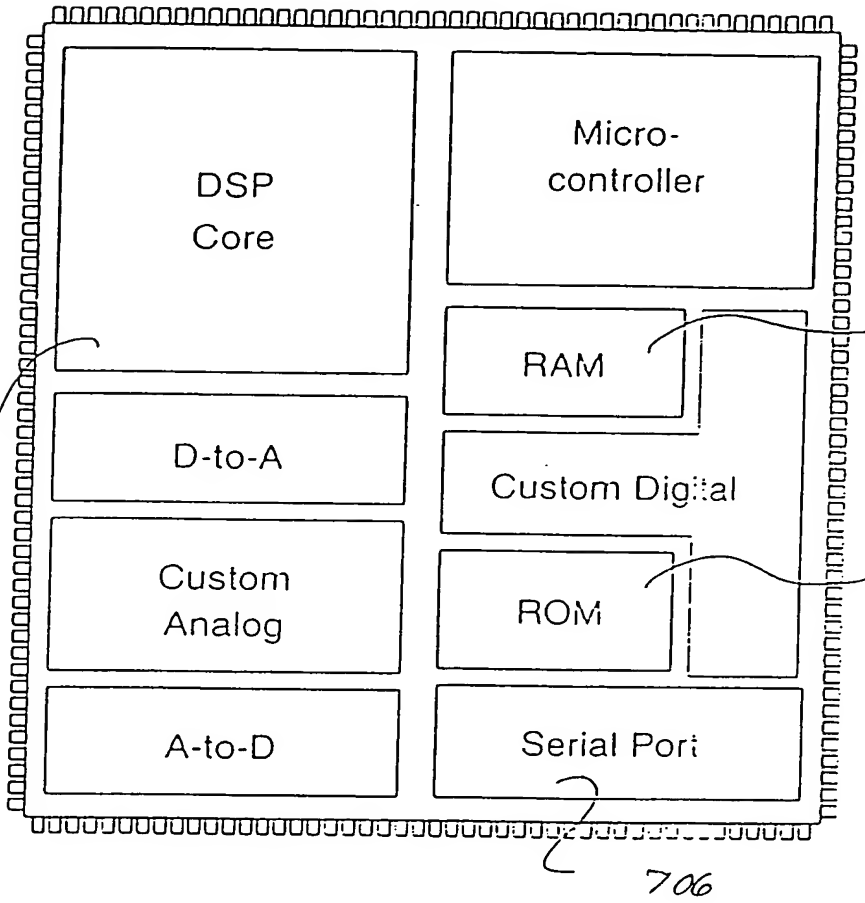

DSP
Core
Micro-
controller
RAM
D-to-A
Custom Digital
Custom
Analog
ROM
A-to-D
Serial Port
700
702
704
704
706

FIG. 7

F.G. 8